

Product Features

- 50 – 4000 MHz
- +27 dBm P1dB
- +40 dBm Output IP3
- High Drain Efficiency
- 20.5 dB Gain @ 900 MHz
- MTTF >100 Years
- SOT-89 SMT Package

Applications

- Mobile Infrastructure
- CATV / DBS
- W-LAN / ISM
- RFID
- Defense / Homeland Security
- Fixed Wireless

Specifications

DC Parameter	Units	Min	Typ	Max
Saturated Drain Current, I_{DSS} (1)	mA	220	290	360
Transconductance, G_m	mS		155	
Pinch Off Voltage, V_p (2)	V		-2.1	
Thermal Resistance	°C / W			68
Junction Temperature (3)	°C			160

RF Parameter (4)	Units	Min	Typ	Max
Frequency Range	MHz	50	900	4000
Small Signal Gain	dB		20.5	
SS Gain (50 Ω , unmatched)	dB	17		21
Maximum Stable Gain	dB		24	
Output P1dB	dBm		+27.4	
Output IP3 (5)	dBm		+40	
Noise Figure	dB		2.7	

1. I_{DSS} is measured with $V_{GS} = 0$ V, $V_{DS} = 3$ V.
2. Pinch-off voltage is measured when $I_{DS} = 1.2$ mA.
3. The junction temperature ensures a minimum MTTF rating of 1 million hours of usage.
4. Test conditions unless otherwise noted: $T = 25^\circ\text{C}$, $V_{DS} = 8$ V, $I_{DQ} = 125$ mA, frequency = 900 MHz in a tuned application circuit with $Z_L = Z_{LOPT}$, $Z_S = Z_{SOPT}$ (optimized for output power).
5. 3OIP measured with two tones at an output power of +12 dBm/tones separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +125 °C
DC Power	2.0 W
RF Input Power (continuous)	6 dB above Input P1dB
Drain to Gate Voltage, V_{DG}	+14 V
Junction Temperature	+220 °C

Operation of this device above any of these parameters may cause permanent damage.

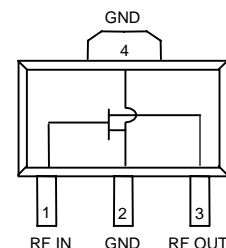
Product Description

The FP1189 is a high performance 1/2-Watt HFET (Heterostructure FET) in a low-cost SOT-89 surface-mount package. This device works optimally at a drain bias of +8 V and 125 mA to achieve +40 dBm output IP3 performance and an output power of +27 dBm at 1-dB compression, while providing 20.5 dB gain at 900 MHz.

The device conforms to WJ Communications' long history of producing high reliability and quality components. The FP1189 has an associated MTTF of greater than 100 years at a mounting temperature of 85°C. All devices are 100% RF & DC tested.

The product is targeted for use as driver amplifiers for wireless infrastructure where high performance and high efficiency are required.

Functional Diagram



Function	Pin No.
Input / Gate	1
Output / Drain	3
Ground	2, 4

Typical Performance

Parameter (6)	Units	Typical		
Frequency	MHz	915	1960	2140
S_{21}	dB	20.6	15.7	14.7
S11	dB	-13	-26	-24
S22	dB	-6.0	-9.6	-9.0
Output P1dB	dBm	+27.4	+27.2	+27.2
Output IP3	dBm	+39.9	+40.4	+39.7
Noise Figure	dB	2.7	3.7	4.3
Channel Power (7) @ -45 dBc ACPR	dBm	+21	+20.8	+18.4
Drain Voltage	V		+8	
Drain Current	mA		125	

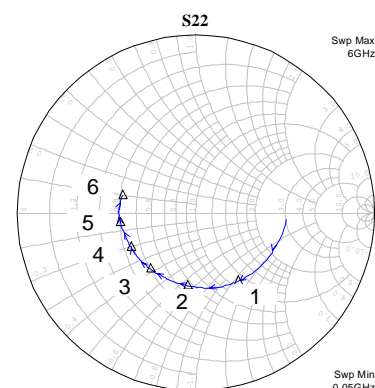
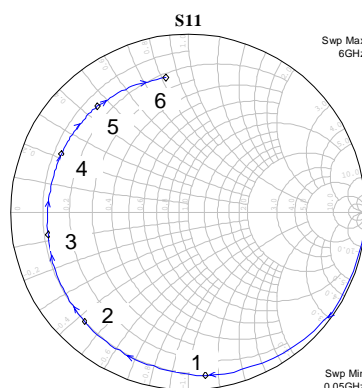
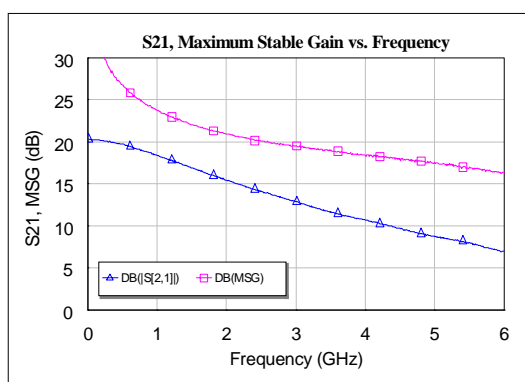
6. Typical parameters represent performance in an application circuit.
7. An IS-95 signal is used for 915 / 1960 MHz. A 3GPP W-CDMA signal is used for 2140 MHz.

Ordering Information

Part No.	Description
FP1189	1/2 -Watt HFET
FP1189-PCB900S	870 – 960 MHz Application Circuit
FP1189-PCB1900S	1930 – 1990 MHz Application Circuit
FP1189-PCB2140S	2110 – 2170 MHz Application Circuit

Typical Device Data

S-Parameters ($V_{DS} = +8\text{ V}$, $I_{DS} = 125\text{ mA}$, $T = 25^\circ\text{C}$, calibrated to device leads)



Note:

Measurements were made on the packaged device in a test fixture with 50 ohm input and output lines.

The S-parameters shown are the de-embedded data down to the device leads and represents typical performance of the device.

Freq (MHz)	S11 (mag)	S11 (ang)	S21 (mag)	S21 (ang)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)
50	1.000	-4.52	10.313	176.55	0.002	87.44	0.544	-3.02
250	0.988	-21.51	10.120	163.88	0.010	76.64	0.535	-13.77
500	0.959	-42.21	9.681	148.45	0.020	64.73	0.520	-27.13
750	0.933	-61.23	9.005	134.71	0.028	53.45	0.495	-39.31
1000	0.895	-78.75	8.270	122.08	0.035	44.25	0.469	-50.54
1250	0.860	-95.09	7.561	109.58	0.040	34.30	0.447	-60.96
1500	0.848	-109.61	7.028	99.15	0.044	26.69	0.428	-70.64
1750	0.821	-122.91	6.408	88.96	0.046	19.57	0.407	-79.82
2000	0.807	-135.32	5.950	79.64	0.048	13.93	0.400	-88.93
2250	0.796	-147.01	5.474	70.37	0.049	7.21	0.386	-97.59
2500	0.785	-157.00	5.087	62.43	0.050	2.99	0.374	-105.24
2750	0.780	-166.26	4.732	53.97	0.050	-1.58	0.376	-113.47
3000	0.775	-175.87	4.415	45.54	0.049	-6.79	0.369	-121.84
3250	0.766	175.78	4.082	38.18	0.049	-9.36	0.368	-129.77
3500	0.770	167.34	3.843	30.76	0.048	-12.48	0.372	-137.25
3750	0.771	159.87	3.602	23.91	0.050	-14.97	0.369	-144.61
4000	0.771	152.07	3.408	16.74	0.050	-17.53	0.374	-152.17
4250	0.771	145.63	3.241	9.15	0.048	-19.53	0.382	-161.00
4500	0.772	138.97	3.053	2.49	0.048	-21.27	0.387	-168.31
4750	0.770	132.07	2.876	-4.50	0.050	-23.00	0.396	-175.08
5000	0.780	126.56	2.743	-10.47	0.048	-25.08	0.408	177.65
5250	0.794	120.21	2.622	-17.28	0.049	-26.64	0.412	170.89
5500	0.795	114.22	2.507	-24.43	0.051	-30.44	0.423	162.41
5750	0.794	108.27	2.346	-31.21	0.052	-30.16	0.442	154.66
6000	0.798	102.86	2.237	-36.95	0.052	-31.18	0.446	147.41

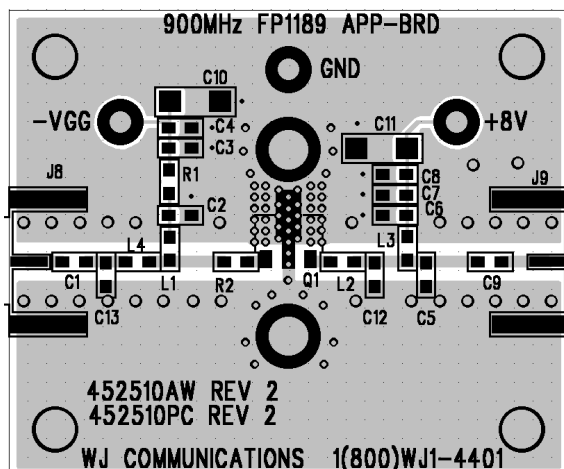
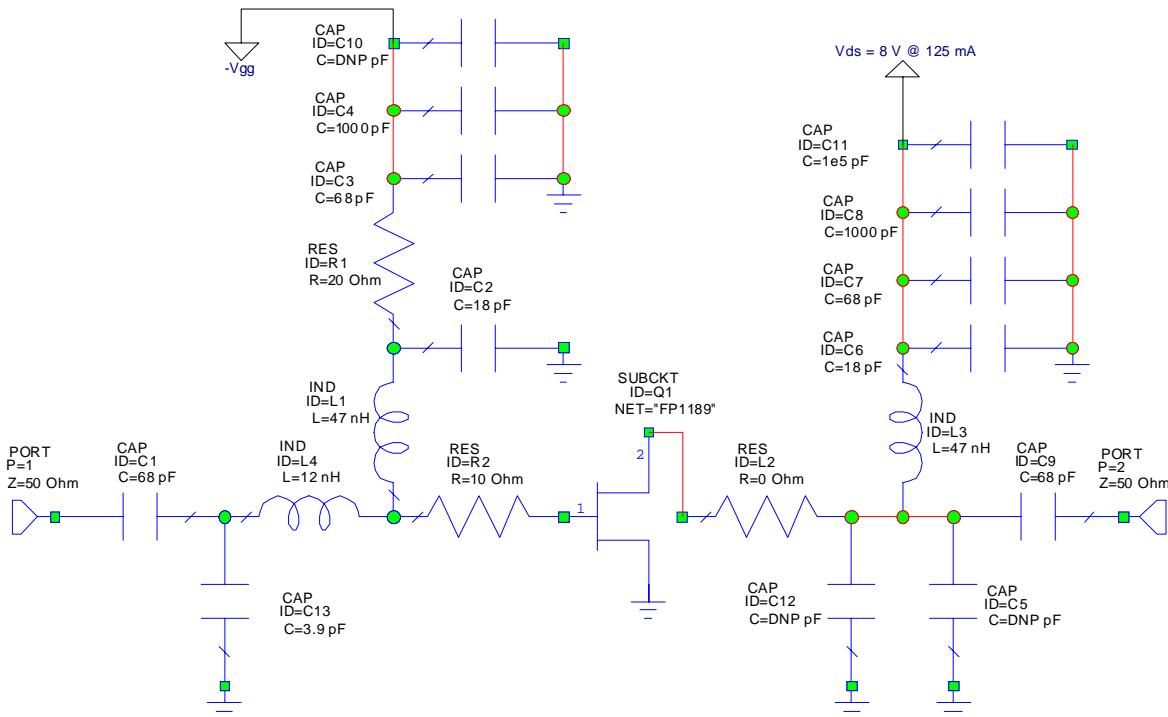
Device S-parameters are available for download off of the website at: <http://www.wj.com>

Application Circuit: 870 – 960 MHz (FP1189-PCB900S)

The application circuit is matched for output power.

Typical RF Performance Drain Bias = +8 V, $I_{ds} = 125$ mA, 25°C

Frequency	MHz	870	915	960
S21 – Gain	dB	20.9	20.6	19.8
S11 – Input Return Loss	dB	-10	-13	-10
S22 – Output Return Loss	dB	-5.2	-6.0	-7.6
Output P1dB	dBm	+27.5	+27.4	+27.5
Output IP3 (+12 dBm / tone, 1 MHz spacing)	dBm		+39.9	
Noise Figure	dB	2.7	2.7	2.6
IS-95 Channel Power @ -45 dBc ACPR	dBm		+21	



Bill of Materials

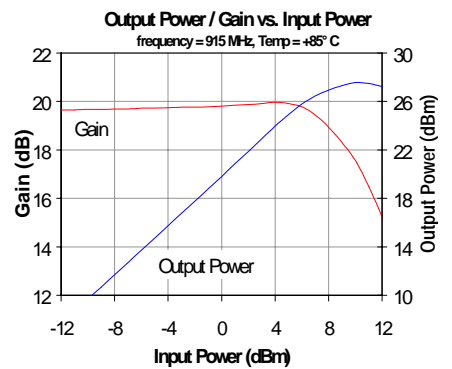
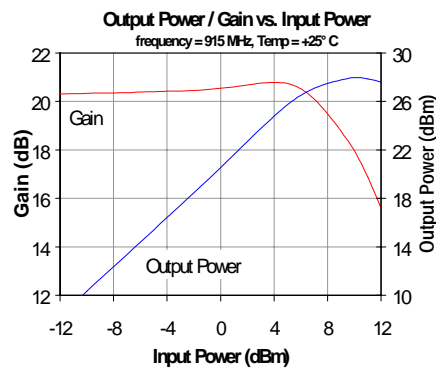
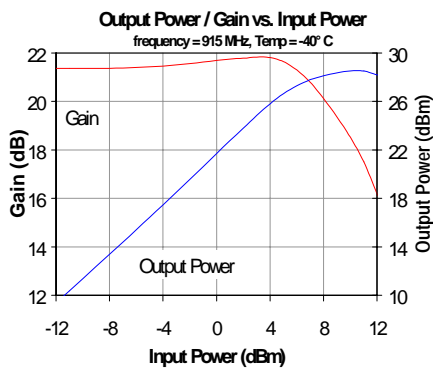
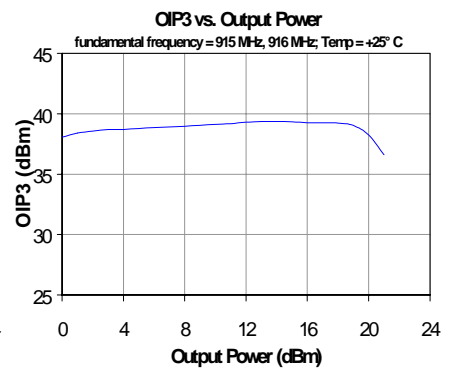
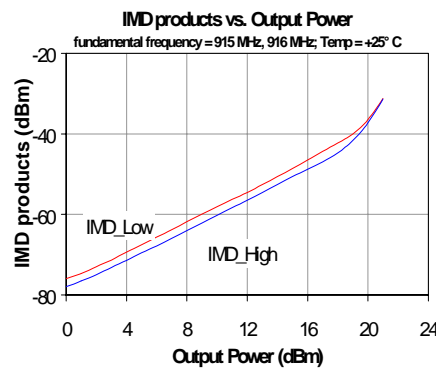
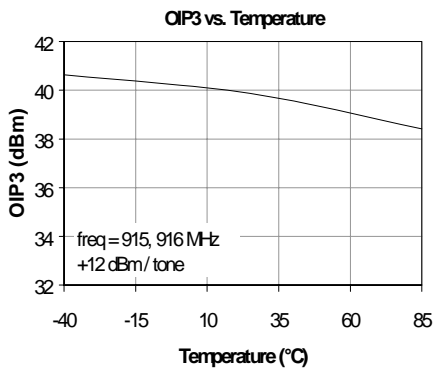
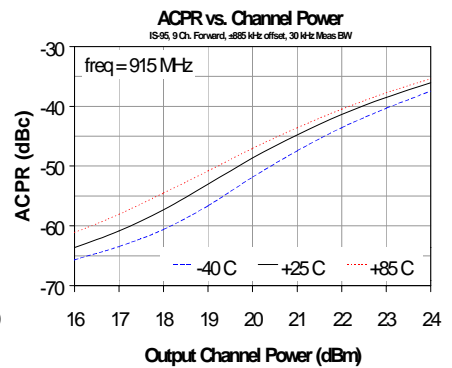
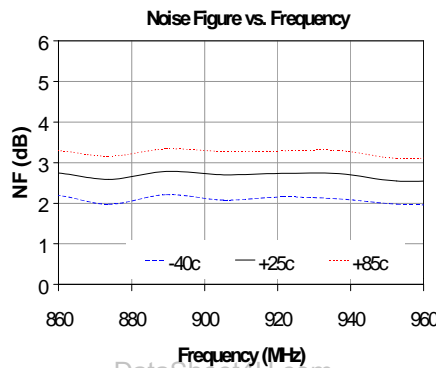
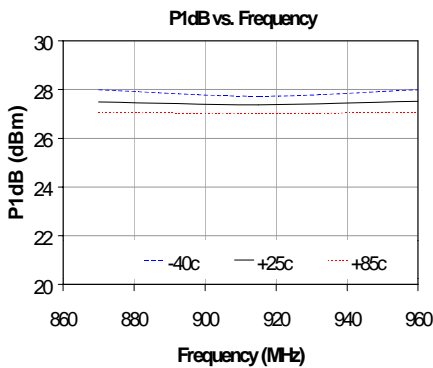
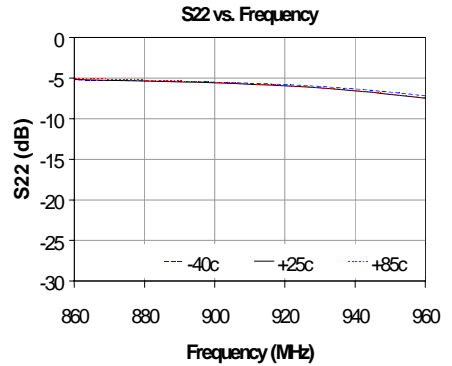
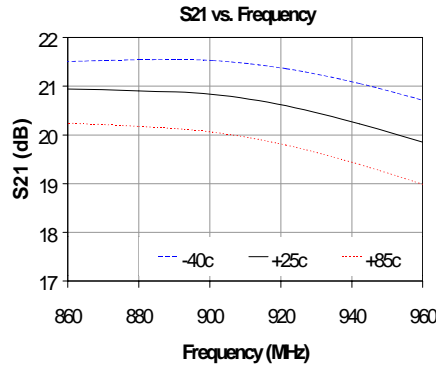
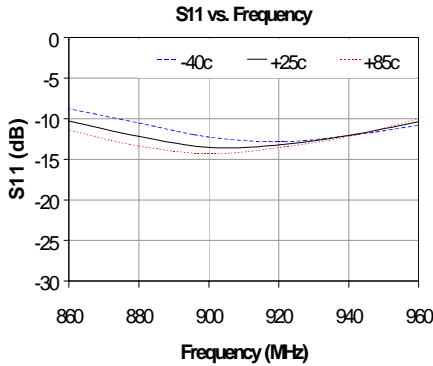
Ref. Desig.	Value	Part style	Size
C1, C3, C7, C9	68 pF	Chip capacitor	0603
C2, C6	18 pF	Chip capacitor	0603
C4, C8	1000 pF	Chip capacitor	0603
C11	0.1 μ F	Chip capacitor	1206
C13	3.9 pF	Chip capacitor	0603
L1, L3	47 nH	Multilayer chip inductor	0603
L2	0 Ω	Chip resistor	0603
L4	12 nH	Multilayer chip inductor	0603
R1	10 Ω	Chip resistor	0603
R2	20 Ω	Chip resistor	0603
Q1	FP1189	WJ 0.5W HFET	SOT-89
C5, C12, C10		Do Not Place	

14 mil GETEK™ ML200DSS ($\epsilon_r = 4.2$)

The main microstrip line has a line impedance of 50 Ω .

Specifications and information are subject to change without notice.

FP1189-PCB900S Application Circuit Performance Plots

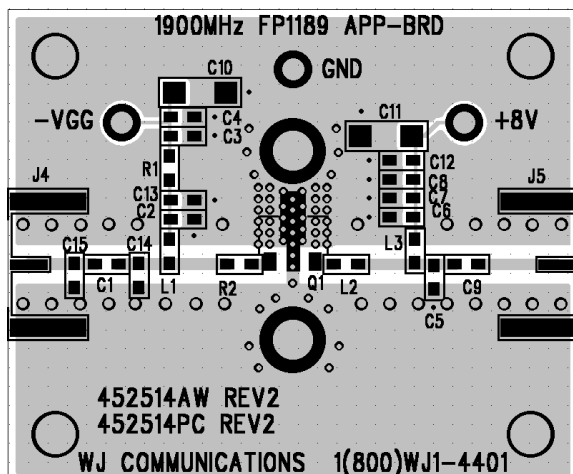
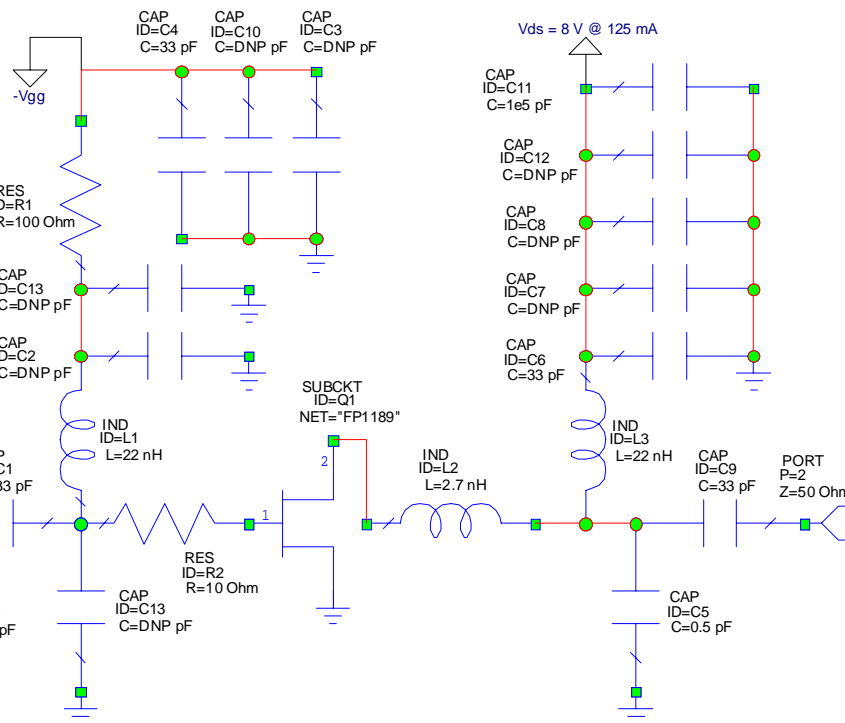


Application Circuit: 1930 – 1990 MHz (FP1189-PCB1900S)

The application circuit is matched for output power.

Typical RF Performance Drain Bias = +8 V, $I_{ds} = 125$ mA, 25°C

Frequency	MHz	1930	1960	1990
S21 – Gain	dB	15.8	15.7	15.5
S11 – Input Return Loss	dB	-26	-26	-24
S22 – Output Return Loss	dB	-9.2	-9.6	-9.0
Output P1dB	dBm	+27.4	+27.2	+27.4
Output IP3 (+12 dBm / tone, 1 MHz spacing)	dBm		+40.4	
Noise Figure	dB		3.7	
IS-95 Channel Power @ -45 dBc ACPR	dBm		+20.8	



Bill of Materials

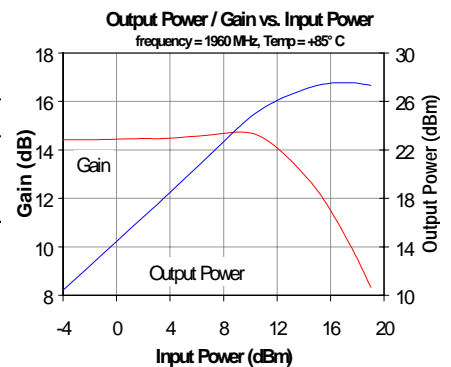
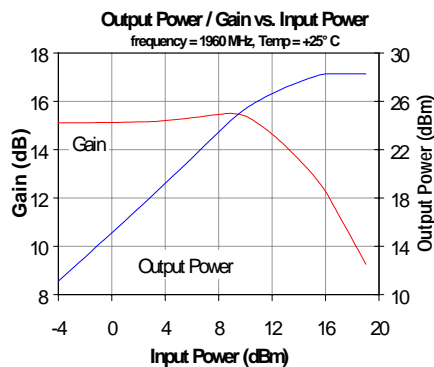
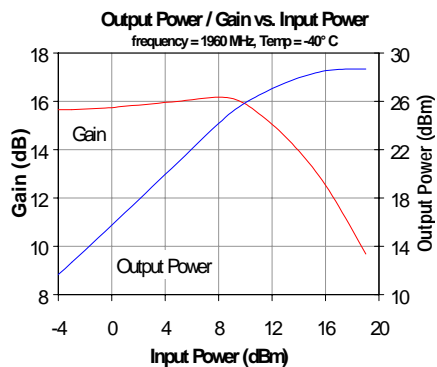
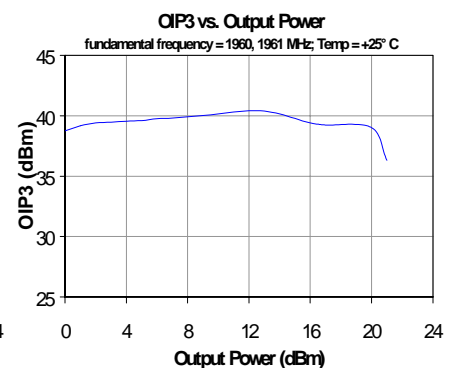
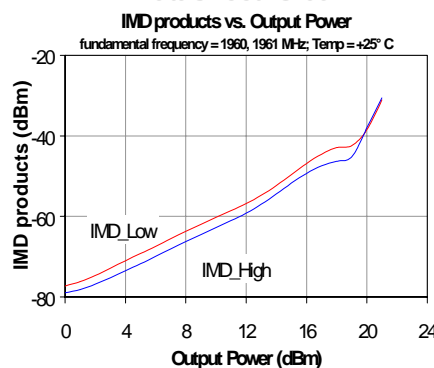
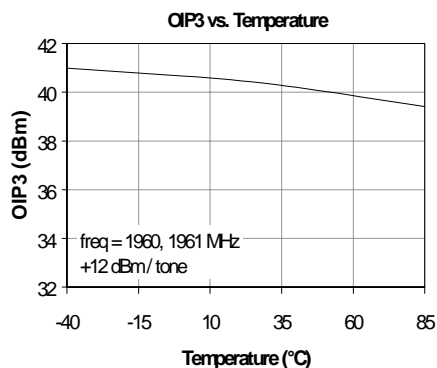
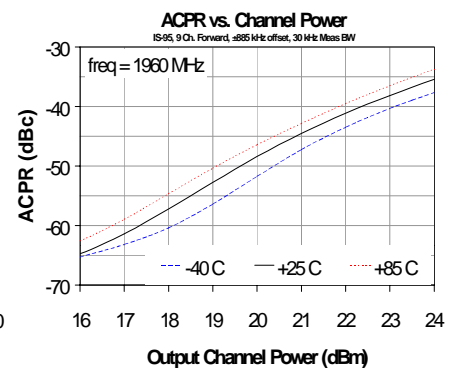
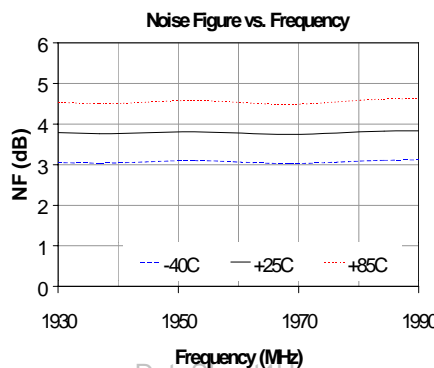
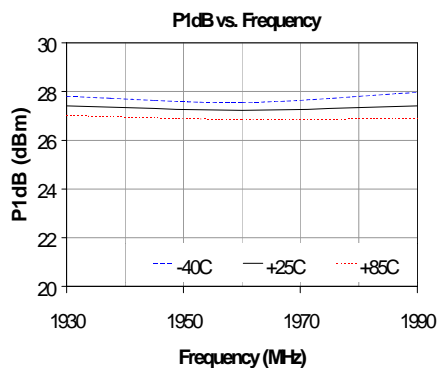
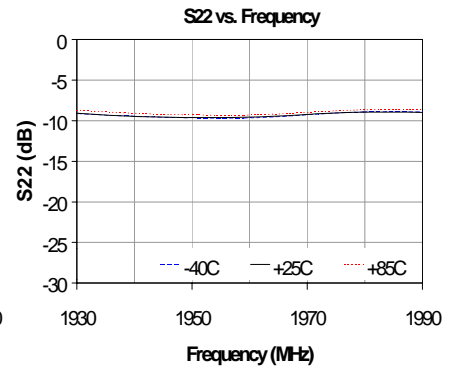
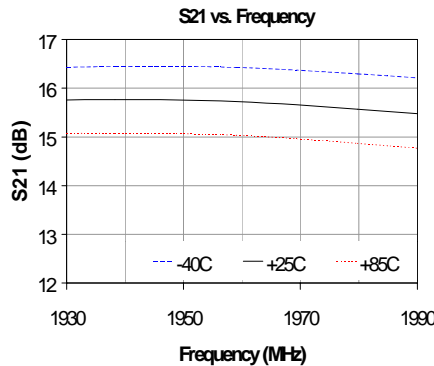
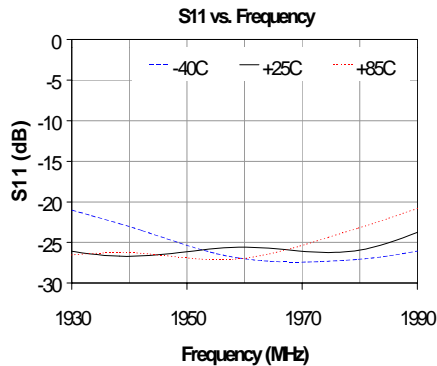
Ref. Desig.	Value	Part style	Size
C1, C4, C6, C9	33 pF	Chip capacitor	0603
C5	0.5 pF	Chip capacitor	0603
C11	0.1 μF	Chip capacitor	1206
C15	1.8 pF	Chip capacitor	0603
L1, L3	22 nH	Multilayer chip inductor	0603
L2	2.7 nH	Multilayer chip inductor	0603
R1	100 Ω	Chip resistor	0603
R2	10 Ω	Chip resistor	0603
Q1	FP1189	WJ 0.5W HFET	SOT-89
C2, C3, C7, C8, C10, C12, C13, C14		Do Not Place	

14 mil GETEKT™ ML200DSS (er = 4.2)
The main microstrip line has a line impedance of 50 Ω.

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Specifications and information are subject to change without notice.

FP1189-PCB1900S Application Circuit Performance Plots

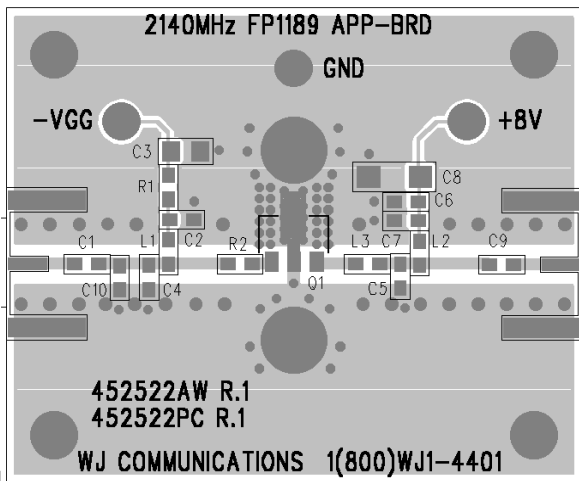
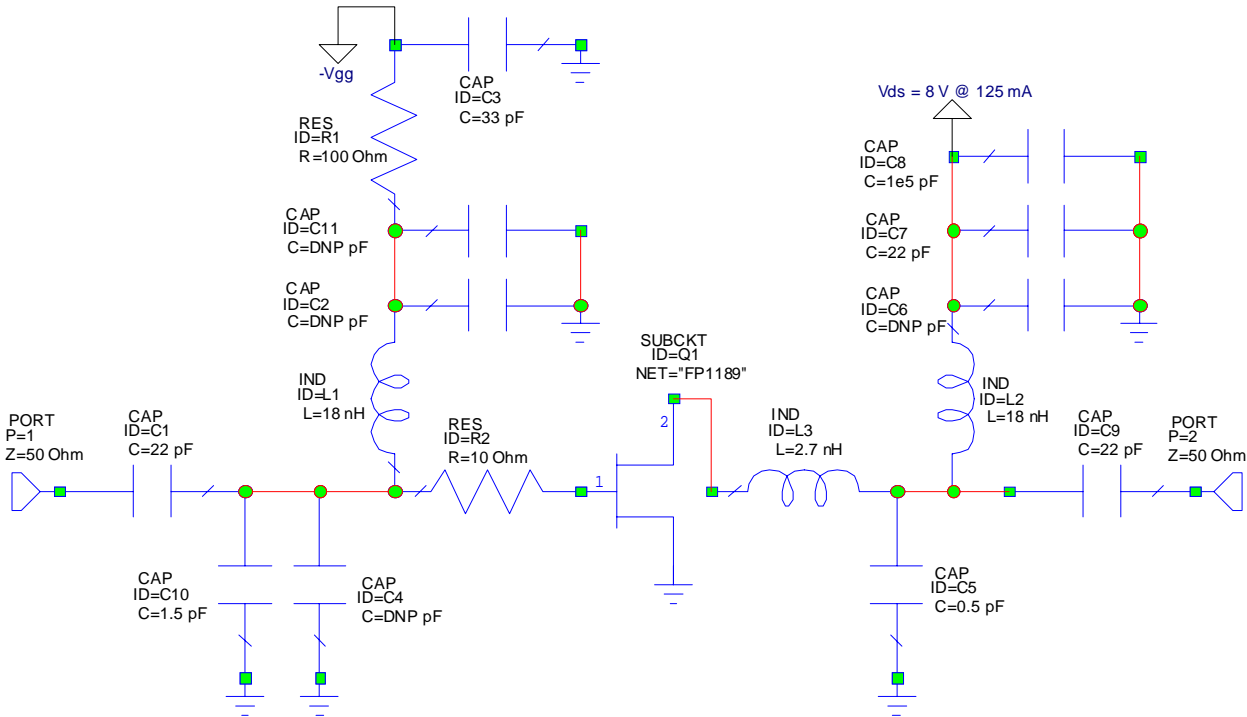


Application Circuit: 2110 – 2170 MHz (FP1189-PCB2140S)

The application circuit is matched for output power.

Typical RF Performance
 Drain Bias = +8 V, $I_{ds} = 125$ mA, 25°C

Frequency	MHz	2110	2140	2170
S21 – Gain	dB	14.7	14.7	14.7
S11 – Input Return Loss	dB	-24	-24	-24
S22 – Output Return Loss	dB	-7.6	-9.0	-9.8
Output P1dB	dBm	+27.1	+27.2	+26.8
Output IP3 (+12 dBm / tone, 1 MHz spacing)	dBm		+39.7	
Noise Figure	dB	4.2	4.3	4.2
W-CDMA Channel Power @ -45 dBc ACPR	dBm		+18.4	

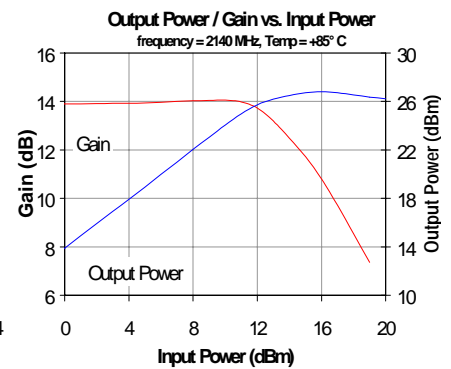
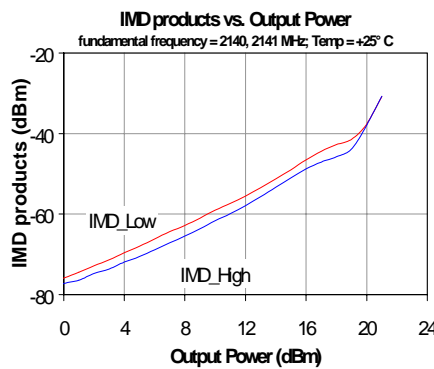
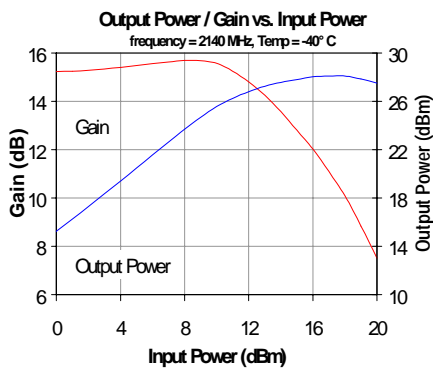
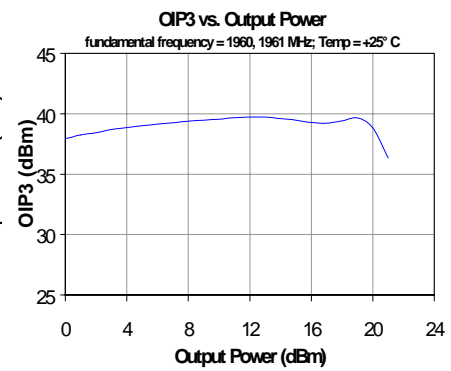
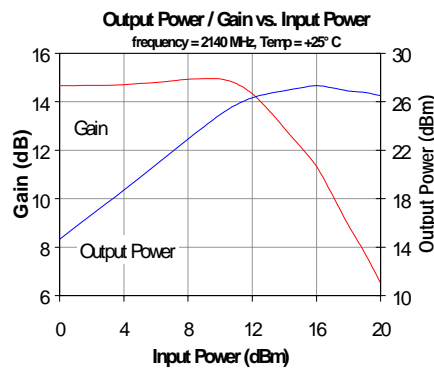
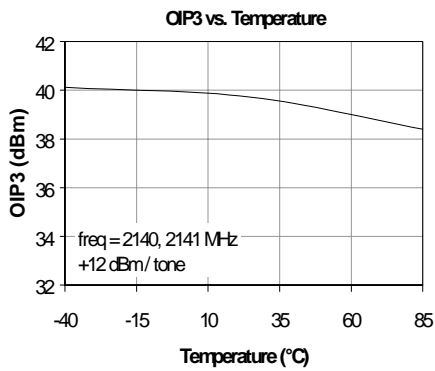
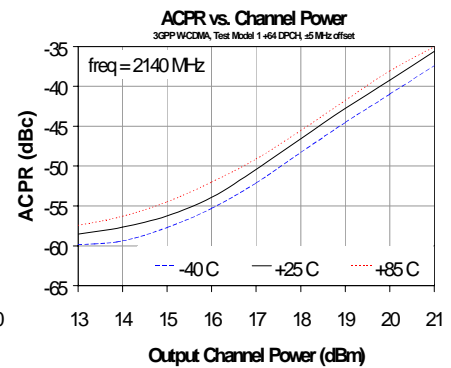
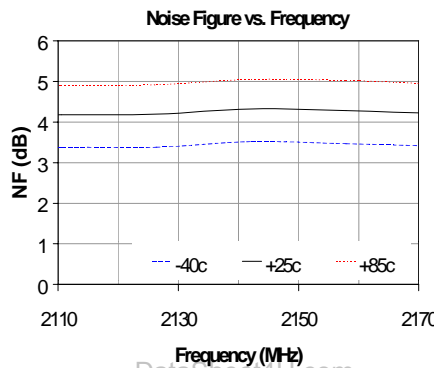
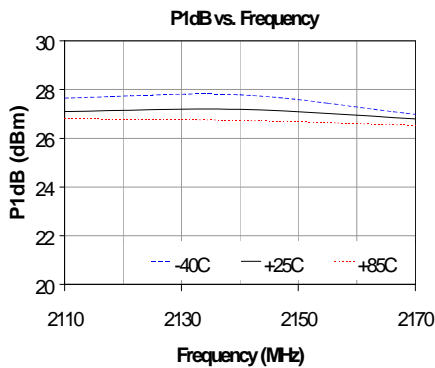
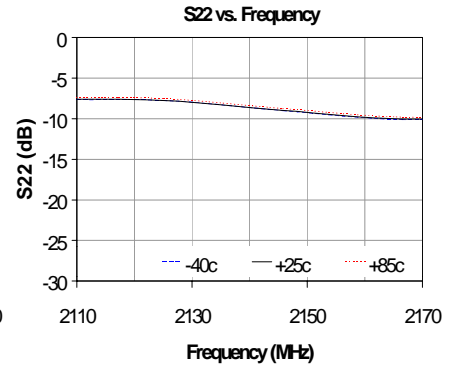
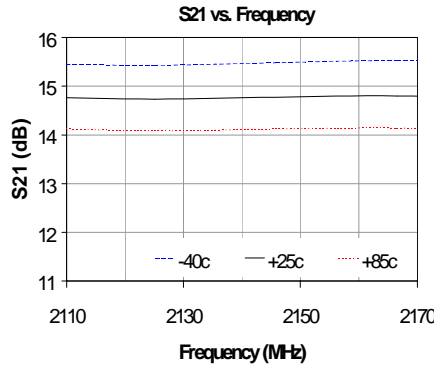
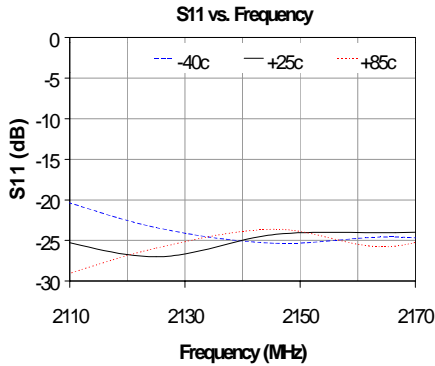


Bill of Materials			
Ref. Desig.	Value	Part style	Size
C1, C7, C9	22 pF	Chip capacitor	0603
C3	33 pF	Chip capacitor	0805
C5	0.5 pF	Chip capacitor	0603
C8	0.1 uF	Chip capacitor	1206
C10	1.5 pF	Chip capacitor	0603
L1, L2	18 nH	Multilayer chip inductor	0603
L3	2.7 nH	Multilayer chip resistor	0603
R1	100 Ohm	Chip resistor	0603
R2	10 Ohm	Chip resistor	0603
Q1	FP1189	WJ 0.5W HFET	SOT-89
C2, C4, C6, C11		Do Not Place	

14 mil GETEK™ ML200DSS ($\epsilon_r = 4.2$)
 The main microstrip line has a line impedance of 50 Ohm.

Specifications and information are subject to change without notice.

FP1189-PCB2140S Application Circuit Performance Plots



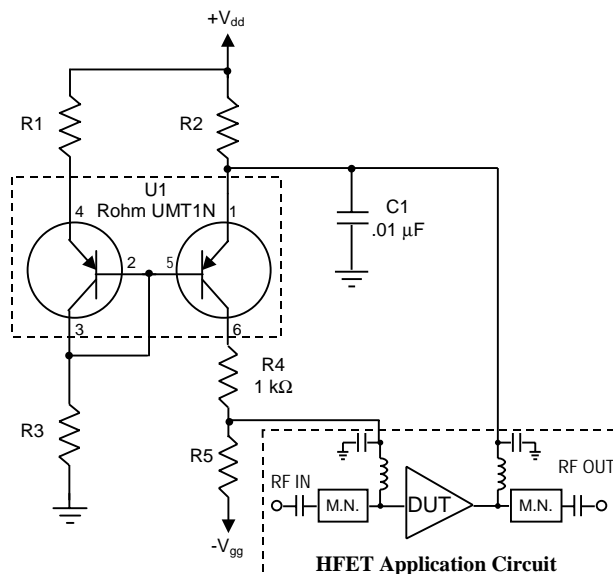
Application Note: Constant-Current Active-Biasing

Special attention should be taken to properly bias the FP1189. Power supply sequencing is required to prevent the device from operating at 100% I_{dss} for a prolonged period of time and possibly causing damage to the device. It is recommended that for the safest operation, the negative supply be “first on and last off.” With a negative gate voltage present, the drain voltage can then be applied to the device. The gate voltage can then be adjusted to have the device be used at the proper quiescent bias condition.

An optional active-bias current mirror is recommended for use with the application circuits shown in this datasheet. Generally in a laboratory environment, the gate voltage is adjusted until the drain draws the recommended operating current. The gate voltage required can vary slightly from device to device because of device pinchoff variation, while also varying slightly over temperature.

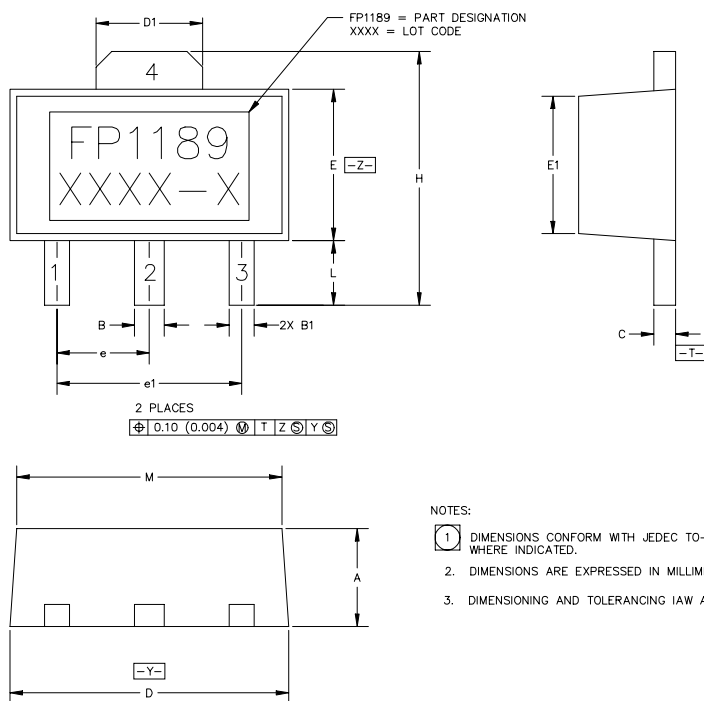
The active-bias circuit, shown on the right, uses dual PNP transistors to provide a constant drain current into the FP1189, while also eliminating the effects of pinchoff variation. This configuration is best suited for applications where the intended output power level of the amplifier is backed off at least 6 dB away from its compression point. With the implementation of the circuit, lower P1dB values may be measured for a Class-AB amplifier, where the device will attempt to source more drain current while the circuit tries to provide a constant drain current. The circuit should be connected directly in line with where the voltage supplies would be normally connected with the amplifier circuit, as shown the diagram. Any required matching circuitry remains the same, although it is not shown in the diagram. This recommended active-bias constant-current circuit adds 7 components to the parts count for implementation, but should cost only an extra \$0.144 to realize (\$0.10 for U1, \$0.0029 for R1, R3, R4, R5, \$0.024 for R2, and \$0.0085 for C1).

Temperature compensation is achieved by tracking the voltage variation with the temperature of the emitter-to-base junction of the two PNP transistors. As a 1st order approximation, this is achieved by using matched transistors with approximately the same I_{be} current. Thus the transistor emitter voltage adjusts the HFET gate voltage so that the device draws a constant current, regardless of the temperature. A Rohm dual transistor - UMT1N - is recommended for cost, minimal board space requirements, and to minimize the variation between the two transistors. Minimizing the variability between the base-to-emitter junctions allow more accuracy in setting the current draw. More details can be found in a separate application note “Active-bias Constant-current Source Recommended for HFETs” found on the WJ website.

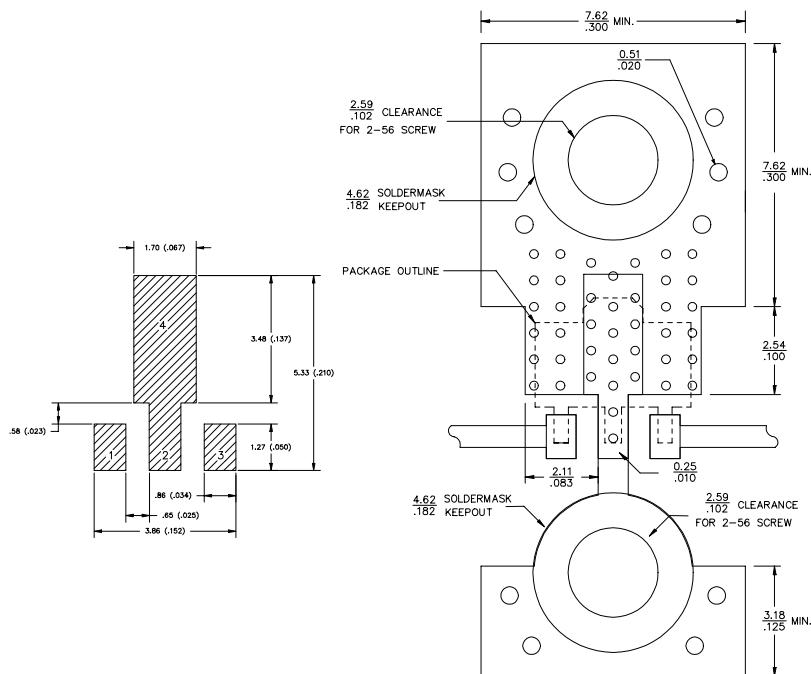


Parameter	FP1189
Pos Supply, V _{dd}	+8 V
Neg Supply, V _{gg}	-5 V
V _{ds}	+7.75 V
I _{ds}	125 mA
R1	62 Ω
R2	2.0 Ω
R3	1.8 kΩ
R4	1 kΩ
R5	1 kΩ

Outline Drawing



Land Pattern



Product Marking

The component will be marked with an "FP1189" designator with a four- or five-digit alphanumeric lot code on the top surface of the package. Tape and reel specifications for this part is located on the website in the "Application Notes" section.

SYMBOL	MIN	MAX
A	1.40 (.055)	1.60 (.063)
B	.44 (.017)	.56 (.022)
B1	.36 (.014)	.48 (.019)
C	.35 (.014)	.44 (.017)
D	4.40 (.173)	4.60 (.181)
D1	1.62 (.064)	1.83 (.072)
E	2.29 (.090)	2.60 (.102)
E1	2.01 (.079)	2.29 (.090)
e	1.50 BSC (.059)	
e1	3.00 BSC (.118)	
H	3.94 (.155)	4.25 (.167)
L	.89 (.035)	1.20 (.047)
M	4.04 (.159)	4.19 (.165)

ESD / MSL Information



Caution! ESD sensitive device.

ESD Classification: Class 1B
 Value: Passes at 800 V
 Test: Human Body Model (HBM)
 Standard: JEDEC Standard JESD22-A114

ESD Classification: Class IV
 Value: Passes at 2000 V
 Test: Charged Device Model (CDM)
 Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3
 Standard: JEDEC Standard J-STD-020A

Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.